

**LIST OF REFERENCES  
CITED BY APPLICANT**

(Use several sheets if necessary)

Atty. Docket No.  
END920030125US1 (17131)

Serial No. 10/821,606  
Unassigned

Applicant  
Sang H. Dhong, et al.

Filing Date  
Herewith 04/08/04

Group  
Unassigned 2195

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
CD	AA	2003/0065698 A1	4/3/03	Ford			
	AB	4,800,516	1/24/89	Si, et al.			
	AC	5,880,983	3/9/99	Elliott, et al.			
	AD	5,940,311	8/17/99	Dao, et al.			
	AE	6,029,243	2/22/00	Pontius, et al.			
	AF	6,044,391	3/28/00	Chao, et al.			
	AG	6,122,721	9/19/00	Goddard, et al.			
CD	AH	6,405,231 B1	6/11/02	Nowka, et al.			
	AI						

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

**OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

CD		Lecce, et al., "A VLSI Implementation of a Novel Bit-Serial Butterfly Processor for FFT", <i>IEEE</i> , Pages 875-879 - 1991;
CD		Luo, et al., "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware With Delayed Addition Techniques, <i>IEEE Transactions On Computers</i> , Vol. 49, No. 3; Pages 208-218 - March 2000;
CD		Yingchun, et al., "A High Speed Microprocessor Core for the Embedded Applications", <i>IEEE</i> , Pages 748-751 - 2001;

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DATE CONSIDERED

07/12/07

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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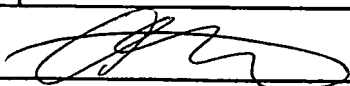
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CD		Enriquez, et al., "Design of a Multi-Mode Pipelined Multiplier for Floating-Point Applications", Air Force Institute of Technology, Pages 77-81 - February 5, 1991;
CD		Inui, et al., "A 250MHz CMOS Floating-Point Divider with Operand Pre-Scaling", Symposium on VLSI Circuits Digest of Technical Papers", Pages 17 and 18 - 1999;
CD		Lee, et al., "MARS- A RISC-based Architecture for LISP", IEEE, Pages 198-206 - 1984; and

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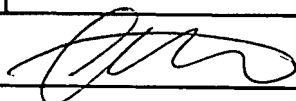
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CD		Namjoo, et al., "CMOS Gate Array Implementation of the Sparc Architecture", IEEE, Pages 10-13 - 1988.

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